

Search History

STN

(HAPPUS, INSPEC, JPAT20, USPATALL, INPADOC)

4/25/86

=> d 17 1-2 abs,bib

L7 ANSWER 1 OF 2 USPATFULL on STN

AB The present invention provides a silicon epitaxial wafer having an excellent ¹⁵ capability all over the radial direction thereof and a process for manufacturing the same. The present invention is applied to a silicon epitaxial wafer having an excellent gettering capability all over the radial direction thereof, wherein density of oxide precipitates detectable in the interior of a silicon single crystal substrate after epitaxial growth is 1×10^{10} sup.9/cm² sup.8 or higher at any position in the radial direction.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2005:102905 USPATFULL
TI Silicon epitaxial wafer and its production method
IN Takeno, Hiroshi, Annaka-shi Gunma, JAPAN
PI US 2005087830 A1 20050428
AI US 2003-501672 A1 20030117 (10)
WO 2003-JP345 20030117
PRAI JP 2002-16663 20020125
DT Utility
FS APPLICATION
LREP WENDEROTH, LIND & PONACK, L.L.P., 2033 K STREET N. W., SUITE 800, WASHINGTON, DC, 20006-1021, US
CLMN Number of Claims: 6
ECL Exemplary Claim: 1
DRWN 2 Drawing Page(s)
LN.CNT 493

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L7 ANSWER 2 OF 2 INPADOC COPYRIGHT 2006 EPO on STN

LEVEL 1

AN 271912375 INPADOC ED 20050519 EW 200520 UP 20050519 UW 200520
TI Silicon epitaxial wafer and its production method.
IN TAKENO HIROSHI
INS TAKENO HIROSHI
INA JP
PA TAKENO HIROSHI
PAS TAKENO HIROSHI
PAA JP
TL English
LA English
DT Patent
PIT USAA PATENT APPLICATION PUBLICATION (PRE-GRANT)
PI US 2005087830 AA 20050428
AI US 2004-501672 A 20040716
PRAI JP 2002-16663 A 20020125 (EDPR 20030901)
WO 2003-JP345 W 20030117 (EDPR 20041111)

=> d 19 1-2 abs,bib

L9 ANSWER 1 OF 2 INSPEC (C) 2006 IET on STN

AN 1994:4679210 INSPEC LN A1994-13-6170T-009; B1994-07-2530F-007
AB To follow the mass transport during annealing of SIMOX structures four <100> single crystal silicon wafers were implanted at 680°C with 90 keV or 70 keV 180+ in order to understand and quantify the effects of the SiO₂ capping layer on the growing buried SiO₂ layer. After implantation pieces of the implanted wafers were capped with 500-1000 nm natural SiO₂

cap by plasma sputtering, and then annealed at 1360°C for 6 h in a quartz silica tube in flowing nitrogen. For the 90 keV wafers (1) 3.5, (2) 4.0, and (3) 4.3+10¹⁷ 180+/cm² the anneal results in continuous oxide layers with some silicon islands and pin holes, and a constant number (1.8+10¹⁷/cm²) of implanted 180 has exchanged with 160 atoms in the cap. The 180 distributions within the cap for the three annealed samples are very similar. The lowest dose (1+10¹⁷ 180+/cm², 70 keV) used for wafer 4 is only about one third of the critical dose (Φ_{CA}) required to form a continuous oxide layer after implantation and annealing. After the anneal, unlike what was found at the higher doses, it is found that all of the implanted 180 has moved to the cap, with no buried oxide precipitate layer being observed. It is proposed that the diffusional exchange of 160 and 180 is thought to be via thermal vacancies. The self-diffusion coefficient of 180 in the SiO₂ cap has been estimated to be between 3.5+10⁻¹⁵ and 3.4+10⁻¹⁴ cm²/s, at 1360°C

AN 1994:4679210 INSPEC DN A1994-13-6170T-009; B1994-07-2530F-007
 TI Oxygen isotopic exchange during the annealing of low energy SIMOX layers
 AU Yupu Li; Kilner, J.A.; Chater, R.J.; (Dept. of Mater., Imperial Coll. of Sci., Technol. & Med., London, UK), Nejim, A.; Hemment, P.L.F.; Marsh, C.D.; Booker, G.R.
 SO Nuclear Instruments & Methods in Physics Research, Section B (Beam Interactions with Materials and Atoms) (March 1994), vol.B85, no.1-4, p. 236-42, 22 refs.
 CODEN: NIMBEU, ISSN: 0168-583X
 Price: 0168-583X/94/\$07.00
 Conference: Ion Beam Analysis. Eleventh International Conference on Ion Beam Analysis, Balatonfured, Hungary, 5-9 July 1993
 DT Conference; Conference Article; Journal
 TC Experimental
 CY Netherlands
 LA English

L9 ANSWER 2 OF 2 INPADOC COPYRIGHT 2006 EPO on STN

LEVEL 1

AN 271912375 INPADOC ED 20050519 EW 200520 UP 20050519 UW 200520
 TI Silicon epitaxial wafer and its production method.
 IN TAKENO HIROSHI
 INS TAKENO HIROSHI
 INA JP
 PA TAKENO HIROSHI
 PAS TAKENO HIROSHI
 PAA JP
 TL English
 LA English
 DT Patent
 PIT USAA PATENT APPLICATION PUBLICATION (PRE-GRANT)
 PI US 2005087830 AA 20050428
 AI US 2004-501672 A 20040716
 PRAI JP 2002-16663 A 20020125 (EDPR 20030901)
 WO 2003-JP345 W 20030117 (EDPR 20041111)

*Applicant's
 Invention*

=> d his

(FILE 'HOME' ENTERED AT 06:10:52 ON 24 JUL 2006)

FILE 'HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2, INPADOC' ENTERED AT 06:11:25 ON 24 JUL 2006

L1 78357 S (SI OR SILICON) (8A) (SINGLE(W)CRYSTAL# OR MONO(W)CRYSTAL#)
 L2 178917 S (SI OR SILICON) (8A) (WAFER#)
 L3 40 S (GETTER?) (8A) (RADIAL OR RADIAL(4A)DIRECTION# OR RADIAL(4A)REG
 L4 13683 S (OXIDE(6A)PRECIPITAT?)

=> d his

(FILE 'HOME' ENTERED AT 06:10:52 ON 24 JUL 2006)

FILE 'HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2, INPADOC' ENTERED AT
06:11:25 ON 24 JUL 2006

L1 78357 S (SI OR SILICON) (8A) (SINGLE(W)CRYSTAL# OR MONO(W)CRYSTAL#)
L2 178917 S (SI OR SILICON) (8A) (WAFER#)
L3 40 S (GETTER?) (8A) (RADIAL OR RADIAL(4A)DIRECTION# OR RADIAL(4A)REG
L4 13683 S (OXIDE(6A)PRECIPITAT?)
L5 191 S (DETECT? OR FIND? OR DISCOVER?) (10A) (INTERIOR(8A)CRYSTAL# OR
L6 74057 S (AFTER?) (10A) (GROW? OR EPITAX?(8A)GROW?)
L7 2 S L1 AND L2 AND L4 AND L5
L8 272 S L1 AND L2 AND L4
L9 2 S L1 AND L2 AND L4 AND L6
L10 2 S L2 AND L3
L11 2 S L2 AND L4 AND L5
L12 53028 S (DOP?) (8A) (BORON)
L13 10824 S L2 AND L12
L14 6440973 S (HEAT? OR ANNEAL?)
L15 38182 S (OXIDIZ?(8A)ATMOSPHERE)
L16 27332 S (STACKING(8A)FAULT#)
L17 15 S L2 AND L4 AND L12 AND L14 AND L15 AND L16
L18 1 S L5 AND L17

=> s 16 and 117

L19 0 L6 AND L17

=> s (getter?)

L20 35264 (GETTER?)

=> s 117 and 120

L21 15 L17 AND L20

=> d 121 1-15 abs,bib

L21 ANSWER 1 OF 15 USPATFULL on STN

AB The present invention is directed to a process for producing a silicon on insulator (SOI) structure having intrinsic gettering, wherein a silicon substrate is subjected to an ideal precipitating wafer heat treatment which enables the substrate, during the heat treatment cycles of essentially any arbitrary electronic device manufacturing process to form an ideal, non-uniform depth distribution of oxygen precipitates, and wherein a dielectric layer is formed beneath the surface of the wafer by implanting oxygen or nitrogen ions, or molecular oxygen, beneath the surface and annealing the wafer. Additionally, the silicon wafer may initially include an epitaxial layer, or an epitaxial layer may be deposited on the substrate during the process of the present invention.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2005:293125 USPATFULL

TI Process for producing silicon on insulator structure having intrinsic gettering by ion implantation

IN Falster, Robert J., London, UNITED KINGDOM

Libbert, Jeffrey L., O'Fallon, MO, UNITED STATES

PA MEMC Electronic Materials, Inc., St. Peters, MO, UNITED STATES, 63376 (non-U.S. corporation)

PI US 2005255671 A1 20051117

~~US 7071080~~ B2 20060704

AI US 2005-174908 A1 20050705 (11)

RLI Division of Ser. No. US 2002-177444, filed on 21 Jun 2002, GRANTED, Pat.

No. US 6930375
PRAI US 2001-337623P 20011205 (60)
US 2001-300208P 20010622 (60)
DT Utility
FS APPLICATION
LREP SENNIGER POWERS LEAVITT AND ROEDEL, ONE METROPOLITAN SQUARE, 16TH FLOOR,
ST LOUIS, MO, 63102, US
CLMN Number of Claims: 42
ECL Exemplary Claim: 1
DRWN 12 Drawing Page(s)
LN.CNT 2106
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L21 ANSWER 2 OF 15 USPATFULL on STN

AB The present invention provides a silicon epitaxial wafer having an excellent IG capability all over the radial direction thereof and a process for manufacturing the same. The present invention is directed to a silicon epitaxial wafer having an excellent gettering capability all over the radial direction thereof wherein density of oxide precipitates detectable in the interior of a silicon single crystal substrate after epitaxial growth is $1+10.\sup{.9}/\text{cm}.\sup{.3}$ or higher at any position in the radial direction.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2005:102905 USPATFULL
TI Silicon epitaxial wafer and its production method
IN Takeno, Hiroshi, Annaka-shi Gunma, JAPAN
PI US 2005087830 A1 20050428
AI US 2003-501672 A1 20030117 (10)
WO 2003-JP345 20030117
PRAI JP 2002-16663 20020125
DT Utility
FS APPLICATION
LREP WENDEROTH, LIND & PONACK, L.L.P., 2033 K STREET N. W., SUITE 800,
WASHINGTON, DC, 20006-1021, US
CLMN Number of Claims: 6
ECL Exemplary Claim: 1
DRWN 2 Drawing Page(s)
LN.CNT 493
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L21 ANSWER 3 OF 15 USPATFULL on STN

AB There are provided silicon single crystal, silicon wafer, and epitaxial wafer having a sufficient gettering effect suitable for a large-scale integrated device. The silicon single crystal which is suitable for an epitaxial wafer is grown with nitrogen doping at a concentration of $1+10.\sup{.13}$ atoms/cm.^{.3} or more, or with nitrogen doping at a concentration of $1+10.\sup{.12}$ atoms/cm.^{.3} and carbon doping at a concentration of $0.1+10.\sup{.16}$ - $5+10.\sup{.16}$ atoms/cm.^{.3} and/or boron doping at a concentration of $1+10.\sup{.17}$ atoms/cm.^{.3} or more. The silicon wafer is produced by slicing from the silicon single crystal, and an epitaxial layer is grown on a surface of the silicon wafer to produce the epitaxial wafer. The present invention provides an epitaxial wafer for a large-scale integrated device having no defects in a device-active region and having an excellent gettering effect without performance of an extrinsic or intrinsic gettering treatment, which is a factor for increasing the number of production steps and production costs.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:277374 USPATFULL

TI Method of making an epitaxial wafer
IN Asayama, Eiichi, Saga-shi, JAPAN
Horai, Masataka, Ogi-gun, JAPAN
Murakami, Hiroki, Ogi-gun, JAPAN
Kubo, Takayuki, Nishinomiya-shi, JAPAN
PI US 2004216659 A1 20041104
AI US 2004-848124 A1 20040519 (10)
RLI Division of Ser. No. US 2003-384534, filed on 11 Mar 2003, PENDING
Continuation of Ser. No. US 2002-55339, filed on 25 Jan 2002, ABANDONED
Continuation of Ser. No. US 1999-362216, filed on 28 Jul 1999, ABANDONED
DT Utility
FS APPLICATION
LREP CLARK & BRODY, 1750 K STREET NW, SUITE 600, WASHINGTON, DC, 20006
CLMN Number of Claims: 4
ECL Exemplary Claim: CLM-01-20
DRWN 8 Drawing Page(s)
LN.CNT 797
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L21 ANSWER 4 OF 15 USPTATFULL on STN
AB There are provided silicon single crystal, silicon wafer, and epitaxial wafer having a sufficient gettering effect suitable for a large-scale integrated device. The silicon single crystal which is suitable for an epitaxial wafer is grown with nitrogen doping at a concentration of 1×10^{13} atoms/cm³ or more, or with nitrogen doping at a concentration of 1×10^{12} atoms/cm³ and carbon doping at a concentration of 0.1×10^{16} to 5×10^{16} atoms/cm³ and/or boron doping at a concentration of 1×10^{17} atoms/cm³ or more. The silicon wafer is produced by slicing from the silicon single crystal, and an epitaxial layer is grown on a surface of the silicon wafer to produce the epitaxial wafer. The present invention provides an epitaxial wafer for a large-scale integrated device having no defects in a device-active region and having an excellent gettering effect without performance of an extrinsic or intrinsic gettering treatment, which is a factor for increasing the number of production steps and production costs.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:250746 USPTATFULL
TI Silicon single crystal, silicon wafer, and epitaxial wafer
IN Asayama, Eiichi, Saga-shi, JAPAN
Horai, Masataka, Ogi-gun, JAPAN
Murakami, Hiroki, Ogi-gun, JAPAN
Kubo, Takayuki, Nishinomiya-shi, JAPAN
PA SUMITOMO METAL INDUSTRIES, LTD., Osaka-shi, JAPAN (non-U.S. corporation)
PI US 2003175532 A1 20030918
US 6878451 B2 20050412
AI US 2003-384534 A1 20030311 (10)
RLI Continuation of Ser. No. US 2002-55339, filed on 25 Jan 2002, ABANDONED
Continuation of Ser. No. US 1999-362216, filed on 28 Jul 1999, ABANDONED
DT Utility
FS APPLICATION
LREP ARMSTRONG, WESTERMAN & HATTORI, LLP, 1725 K STREET, NW, SUITE 1000, WASHINGTON, DC, 20006
CLMN Number of Claims: 20
ECL Exemplary Claim: 1
DRWN 8 Drawing Page(s)
LN.CNT 855
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L21 ANSWER 5 OF 15 USPTATFULL on STN

AB According to the present invention, there is disclosed a silicon single crystal wafer grown according to the CZ method which is a wafer having a diameter of 200 mm or more produced from a single crystal grown at a growth rate of 0.5 mm/min or more without doping except for a dopant for controlling resistance, wherein neither an octahedral void defect due to vacancies nor a dislocation cluster due to interstitial silicons exists as a grown-in defect, and a method for producing it. There can be provided a high quality silicon single crystal wafer having a large diameter wherein a silicon single crystal in which both of octahedral void defects and dislocation clusters which are growth defects are substantially eliminated is grown at higher rate compared with the conventional method by the usual CZ method, and furthermore by controlling a concentrations of interstitial oxygen in the crystal to be low, a precipitation amount is lowered and ununiformity of BMD in a plane of the wafer is improved, and provided a method for producing it.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:156882 USPATFULL
TI Silicon single crystal wafer and method for manufacturing the same
IN Fusegawa, Izumi, Nishishirakawa-gun Fukushima, JAPAN
Kitagawa, Koji, Nishishirakawa-gun Fukushima, JAPAN
Hoshi, Ryoji, Nishishirakawa-gun Fukushima, JAPAN
Sakurada, Masahiro, Nishishirakawa-gun Fukushima, JAPAN
Ohta, Tomohiko, Nishishirakawa-gun Fukushima, JAPAN
PI US 2003106484 A1 20030612
US 6893499 B2 20050517
AI US 2002-312921 A1 20021226 (10)
WO 2001-JP5565 20010628
PRAI JP 2000-199226 20000630
DT Utility
FS APPLICATION
LREP HOGAN & HARTSON L.L.P., 500 S. GRAND AVENUE, SUITE 1900, LOS ANGELES, CA, 90071-2611
CLMN Number of Claims: 7
ECL Exemplary Claim: 1
DRWN 3 Drawing Page(s)
LN.CNT 963
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L21 ANSWER 6 OF 15 USPATFULL on STN

AB The present invention is directed to a process for producing a silicon on insulator (SOI) structure having intrinsic gettering, wherein a silicon substrate is subjected to an ideal precipitating wafer heat treatment which enables the substrate, during the heat treatment cycles of essentially any arbitrary electronic device manufacturing process to form an ideal, non-uniform depth distribution of oxygen precipitates, and wherein a dielectric layer is formed beneath the surface of the wafer by implanting oxygen or nitrogen ions, or molecular oxygen, beneath the surface and annealing the wafer. Additionally, the silicon wafer may initially include an epitaxial layer, or an epitaxial layer may be deposited on the substrate during the process of the present invention.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:10739 USPATFULL
TI Process for producing silicon on insulator structure having intrinsic gettering by ion implantation
IN Falster, Robert J., London, UNITED KINGDOM
Libbert, Jeffrey L., O' Fallon, MO, UNITED STATES
PA MEMC Electronic Materials, Inc. (non-U.S. corporation)
PI US 2003008435 A1 20030109

US 6930375 B2 20050816
AI US 2002-177444 A1 20020621 (10)
PRAI US 2001-300208P 20010622 (60)
US 2001-337623P 20011205 (60)
DT Utility
FS APPLICATION
LREP SENNIGER POWERS LEAVITT AND ROEDEL, ONE METROPOLITAN SQUARE, 16TH FLOOR,
ST LOUIS, MO, 63102
CLMN Number of Claims: 76
ECL Exemplary Claim: 1
DRWN 12 Drawing Page(s)
LN.CNT 2242
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L21 ANSWER 7 OF 15 USPATFULL on STN

AB There are provided silicon single crystal, silicon wafer, and epitaxial wafer having a sufficient gettering effect suitable for a large-scale integrated device. The silicon single crystal which is suitable for an epitaxial wafer is grown with nitrogen doping at a concentration of 1×10^{13} atoms/cm³ or more, or with nitrogen doping at a concentration of 1×10^{12} atoms/cm³ and carbon doping at a concentration of 0.1×10^{16} – 5×10^{16} atoms/cm³ and/or boron doping at a concentration of 1×10^{17} atoms/cm³ or more. The silicon wafer is produced by slicing from the silicon single crystal, and an epitaxial layer is grown on a surface of the silicon wafer to produce the epitaxial wafer. The present invention provides an epitaxial wafer for a large-scale integrated device having no defects in a device-active region and having an excellent gettering effect without performance of an extrinsic or intrinsic gettering treatment, which is a factor for increasing the number of production steps and production costs.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:258602 USPATFULL
TI Silicon single crystal, silicon wafer, and epitaxial wafer
IN Asayama, Eiichi, Saga-shi, JAPAN
Horai, Masataka, Ogi-gun, JAPAN
Murakami, Hiroki, Ogi-gun, JAPAN
Kubo, Takayuki, Nishinomiya-shi, JAPAN
Umeno, Shigeru, Sasebo-shi, JAPAN
Sadamitsu, Shinsuke, Saga-shi, JAPAN
Koike, Yasuo, Kashima-shi, JAPAN
Sueoka, Kouji, Amagasaki-shi, JAPAN
Katahama, Hisashi, Kishima-gun, JAPAN
PA SUMITOMO METAL INDUSTRIES, LTD. (non-U.S. corporation)
PI US 2002142171 A1 20021003
US 6641888 B2 20031104
AI US 2002-55340 A1 20020125 (10)
RLI Division of Ser. No. US 1999-362216, filed on 28 Jul 1999, ABANDONED
DT Utility
FS APPLICATION
LREP ARMSTRONG, WESTERMAN & HATTORI, LLP, 1725 K STREET, NW., SUITE 1000,
WASHINGTON, DC, 20006
CLMN Number of Claims: 20
ECL Exemplary Claim: 1
DRWN 8 Drawing Page(s)
LN.CNT 843
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L21 ANSWER 8 OF 15 USPATFULL on STN

AB There are provided silicon single crystal, silicon

wafer, and epitaxial wafer having a sufficient gettering effect suitable for a large-scale integrated device. The silicon single crystal which is suitable for an epitaxial wafer is grown with nitrogen doping at a concentration of 1×10^{13} atoms/cm³ or more, or with nitrogen doping at a concentration of 1×10^{12} atoms/cm³ and carbon doping at a concentration of 0.1×10^{16} – 5×10^{16} atoms/cm³ and/or boron doping at a concentration of 1×10^{17} atoms/cm³ or more. The silicon wafer is produced by slicing from the silicon single crystal, and an epitaxial layer is grown on a surface of the silicon wafer to produce the epitaxial wafer. The present invention provides an epitaxial wafer for a large-scale integrated device having no defects in a device-active region and having an excellent gettering effect without performance of an extrinsic or intrinsic gettering treatment, which is a factor for increasing the number of production steps and production costs.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:258601 USPTFLL
 TI Silicon single crystal, silicon wafer, and epitaxial wafer
 IN Asayama, Eiichi, Saga-shi, JAPAN
 Horai, Masataka, Ogi-gun, JAPAN
 Murakami, Hiroki, Ogi-gun, JAPAN
 Kubo, Takayuki, Nishinomiya-shi, JAPAN
 Umeno, Shigeru, Sasebo-shi, JAPAN
 Sadamitsu, Shinsuke, Saga-shi, JAPAN
 Koike, Yasuo, Kashima-shi, JAPAN
 Sueoka, Kouji, Amagasaki-shi, JAPAN
 Katahama, Hisashi, Kishima-gun, JAPAN
 PA SUMITOMO METAL INDUSTRIES, LTD. (non-U.S. corporation)
 PI US 2002142170 A1 20021003
 AI US 2002-55339 A1 20020125 (10)
 RLI Continuation of Ser. No. US 1999-362216, filed on 28 Jul 1999, ABANDONED
 DT Utility
 FS APPLICATION
 LREP ARMSTRONG, WESTERMAN & HATTORI, LLP, 1725 K STREET, NW., SUITE 1000, WASHINGTON, DC, 20006
 CLMN Number of Claims: 20
 ECL Exemplary Claim: 1
 DRWN 8 Drawing Page(s)
 LN.CNT 854

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L21 ANSWER 9 OF 15 USPTFLL on STN

AB A silicon wafer characterized in that the laser scattering tomography defect occurrence region accounts for at least 80% of the wafer surface area and that the laser scattering tomography defects have a mean size of not more than 0.1 μ m, with the density of those defects which exceed 0.1 μ m in size being not more than $1 \times 10^{5.5}$ cm⁻³, and wafers derived from this wafer as the raw material by heat treatment for oxide precipitate formation, by heat treatment for denuded layer formation or by epitaxial layer formation on the surface are useful as semiconductor materials. In producing this wafer, a single crystal is pulled up under pulling conditions such that while the temperature of the central portion of the single crystal being pulled up from the melt is within the range from the melting point to 1,370° C., the temperature gradient G.sub.c in the central portion in the single crystal pulling axis direction is not less than 2.8° C./mm and the ratio G.sub.c/G.sub.e, where G.sub.e is the temperature gradient in the peripheral portion in the pulling axis direction, is not less than 1. By doing so, silicon

wafers very low in surface defect density and allowing the uniform and sufficient formation of BMDs can be obtained.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:156842 USPATFULL
TI Silicon wafer and epitaxial silicon wafer utilizing same
IN Murakami, Hiroki, Saga, JAPAN
Egashira, Kazuyuki, Saga, JAPAN
PA Sumitomo Metal Industries, Ltd., Osaka-shi, JAPAN (non-U.S. corporation)
PI US 2002081440 A1 20020627
US 6569535 B2 20030527
AI US 2001-17295 A1 20011218 (10)
PRAI JP 2000-387045 20001220
DT Utility
FS APPLICATION
LREP ARMSTRONG, WESTERMAN & HATTORI, LLP, 1725 K STREET, NW., SUITE 1000, WASHINGTON, DC, 20006
CLMN Number of Claims: 18
ECL Exemplary Claim: 1
DRWN 9 Drawing Page(s)
LN.CNT 972

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L21 ANSWER 10 OF 15 USPAT2 on STN

AB The present invention is directed to a process for producing a silicon on insulator (SOI) structure having intrinsic gettering, wherein a silicon substrate is subjected to an ideal precipitating wafer heat treatment which enables the substrate, during the heat treatment cycles of essentially any arbitrary electronic device manufacturing process to form an ideal, non-uniform depth distribution of oxygen precipitates, and wherein a dielectric layer is formed beneath the surface of the wafer by implanting oxygen or nitrogen ions, or molecular oxygen, beneath the surface and annealing the wafer. Additionally, the silicon wafer may initially include an epitaxial layer, or an epitaxial layer may be deposited on the substrate during the process of the present invention.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2005:293125 USPAT2
TI Process for producing silicon on insulator structure having intrinsic gettering by ion implantation
IN Falster, Robert J., London, UNITED KINGDOM
Libbert, Jeffrey L., O'Fallon, MO, UNITED STATES
PA MEMC Electronic Materials, Inc., St. Peters, MO, UNITED STATES (U.S. corporation)
PI US 7071080 B2 20060704
AI US 2005-174908 20050705 (11)
RLI Division of Ser. No. US 2002-177444, filed on 21 Jun 2002, Pat. No. US 6930375
PRAI US 2001-337623P 20011205 (60)
US 2001-300208P 20010622 (60)
DT Utility
FS GRANTED
EXNAM Primary Examiner: Mai, Anh D.; Assistant Examiner: Trinh, (Vikki) Hoa B.
LREP Senniger Powers
CLMN Number of Claims: 42
ECL Exemplary Claim: 1
DRWN 14 Drawing Figure(s); 12 Drawing Page(s)
LN.CNT 2108

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L21 ANSWER 11 OF 15 USPAT2 on STN

AB There are provided silicon single crystal, silicon wafer, and epitaxial wafer having a sufficient gettering effect suitable for a large-scale integrated device. The silicon single crystal which is suitable for an epitaxial wafer is grown with nitrogen doping at a concentration of 1×10^{13} atoms/cm³ or more, or with nitrogen doping at a concentration of 1×10^{12} atoms/cm³ and carbon doping at a concentration of 0.1×10^{16} – 5×10^{16} atoms/cm³ and/or boron doping at a concentration of 1×10^{17} atoms/cm³ or more. The silicon wafer is produced by slicing from the silicon single crystal, and an epitaxial layer is grown on a surface of the silicon wafer to produce the epitaxial wafer. The present invention provides an epitaxial wafer for a large-scale integrated device having no defects in a device-active region and having an excellent gettering effect without performance of an extrinsic or intrinsic gettering treatment, which is a factor for increasing the number of production steps and production costs.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:250746 USPAT2
TI Silicon single crystal, silicon wafer, and epitaxial wafer
IN Asayama, Eiichi, Saga, JAPAN
Horai, Masataka, Saga, JAPAN
Murakami, Hiroki, Saga, JAPAN
Kubo, Takayuki, Nishinomiya, JAPAN
PA Sumitomo Mitsubishi Silicon Corporation, Tokyo, JAPAN (non-U.S. corporation)
PI US 6878451 B2 20050412
AI US 2003-384534 20030311 (10)
RLI Continuation of Ser. No. US 2002-55339, filed on 25 Jan 2002, ABANDONED
Continuation of Ser. No. US 1999-362216, filed on 28 Jul 1999, ABANDONED
DT Utility
FS GRANTED
EXNAM Primary Examiner: Stein, Stephen
LREP Clark & Brody
CLMN Number of Claims: 3
ECL Exemplary Claim: 2
DRWN 8 Drawing Figure(s); 8 Drawing Page(s)
LN.CNT 797

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L21 ANSWER 12 OF 15 USPAT2 on STN

AB According to the present invention, there is disclosed a silicon single crystal wafer grown according to the CZ method which is a wafer having a diameter of 200 mm or more produced from a single crystal grown at a growth rate of 0.5 mm/min or more without doping except for a dopant for controlling resistance, wherein neither an octahedral void defect due to vacancies nor a dislocation cluster due to interstitial silicons exists as a grown-in defect, and a method for producing it. There can be provided a high quality silicon single crystal wafer having a large diameter wherein a silicon single crystal in which both of octahedral void defects and dislocation clusters which are growth defects are substantially eliminated is grown at higher rate compared with the conventional method by the usual CZ method, and furthermore by controlling a concentrations of interstitial oxygen in the crystal to be low, a precipitation amount is lowered and ununiformity of BMD in a plane of the wafer is improved, and provided a method for producing it.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:156882 USPAT2
TI Silicon single crystal wafer and method for

manufacturing the same
IN Fusegawa, Izumi, Fukushima, JAPAN
Kitagawa, Koji, Fukushima, JAPAN
Hoshi, Ryoji, Fukushima, JAPAN
Sakurada, Masahiro, Fukushima, JAPAN
Ohta, Tomohiko, Fukushima, JAPAN
PA Shin-Etsu Handotai Co., Ltd., Tokyo, JAPAN (non-U.S. corporation)
PI US 6893499 B2 20050517
WO 2002002852 20020110
AI US 2002-312921 20010628 (10)
WO 2001-JP5565 20010628
20021226 PCT 371 date
PRAI JP 2000-199226 20000630
DT Utility
FS GRANTED
EXNAM Primary Examiner: Hiteshew, Felisa
LREP Hogan & Hartson, LLP
CLMN Number of Claims: 11
ECL Exemplary Claim: 1
DRWN 6 Drawing Figure(s); 3 Drawing Page(s)
LN.CNT 983
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L21 ANSWER 13 OF 15 USPAT2 on STN

AB The present invention is directed to a process for producing a silicon on insulator (SOI) structure having intrinsic gettering, wherein a silicon substrate is subjected to an ideal precipitating wafer heat treatment which enables the substrate, during the heat treatment cycles of essentially any arbitrary electronic device manufacturing process to form an ideal, non-uniform depth distribution of oxygen precipitates, and wherein a dielectric layer is formed beneath the surface of the wafer by implanting oxygen or nitrogen ions, or molecular oxygen, beneath the surface and annealing the wafer. Additionally, the silicon wafer may initially include an epitaxial layer, or an epitaxial layer may be deposited on the substrate during the process of the present invention.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:10739 USPAT2
TI Silicon on insulator structure having an epitaxial layer and intrinsic gettering
IN Falster, Robert J., London, UNITED KINGDOM
Libbert, Jeffrey L., O'Fallon, MO, UNITED STATES
PA MEMC Electronic Materials, Inc., St. Peters, MO, UNITED STATES (U.S. corporation)
PI US 6930375 B2 20050816
AI US 2002-177444 20020621 (10)
PRAI US 2001-337623P 20011205 (60)
US 2001-300208P 20010622 (60)
DT Utility
FS GRANTED
EXNAM Primary Examiner: Weiss, Howard; Assistant Examiner: Trinh, (Vikki) Hoa B.
LREP Senniger Powers
CLMN Number of Claims: 34
ECL Exemplary Claim: 1
DRWN 14 Drawing Figure(s); 12 Drawing Page(s)
LN.CNT 2005
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L21 ANSWER 14 OF 15 USPAT2 on STN

AB There are provided silicon single crystal, silicon wafer, and epitaxial wafer having a sufficient

gettering effect suitable for a large-scale integrated device. The silicon single crystal which is suitable for an epitaxial wafer is grown with nitrogen doping at a concentration of 1×10^{13} atoms/cm³ or more, or with nitrogen doping at a concentration of 1×10^{12} atoms/cm³ and carbon doping at a concentration of 0.1×10^{15} – 5×10^{16} atoms/cm³ and/or boron doping at a concentration of 1×10^{17} atoms/cm³ or more. The silicon wafer is produced by slicing from the silicon single crystal, and an epitaxial layer is grown on a surface of the silicon wafer to produce the epitaxial wafer. The present invention provides an epitaxial wafer for a large-scale integrated device having no defects in a device-active region and having an excellent gettering effect without performance of an extrinsic or intrinsic gettering treatment.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:258602 USPAT2
 TI Silicon single crystal, silicon wafer, and epitaxial wafer.
 IN Asayama, Eiichi, Saga, JAPAN
 Horai, Masataka, Saga, JAPAN
 Umeno, Shigeru, Sasebo, JAPAN
 Sadamitsu, Shinsuke, Saga, JAPAN
 Koike, Yasuo, Kashima, JAPAN
 Sueoka, Kouji, Amagasaki, JAPAN
 Katahama, Hisashi, Saga, JAPAN
 PA Sumitomo Mitsubishi Silicon Corporation, Tokyo, JAPAN (non-U.S. corporation)
 PI US 6641888 B2 20031104
 AI US 2002-55340 20020125 (10)
 RLI Division of Ser. No. US 1999-362216, filed on 28 Jul 1999, now abandoned
 PRAI JP 1999-83424 19990326
 DT Utility
 FS GRANTED
 EXNAM Primary Examiner: Jones, Deborah; Assistant Examiner: Stein, Stephen
 LREP Armstrong, Westerman & Hattori, LLP
 CLMN Number of Claims: 12
 ECL Exemplary Claim: 9
 DRWN 8 Drawing Figure(s); 8 Drawing Page(s)
 LN.CNT 798

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L21 ANSWER 15 OF 15 USPAT2 on STN
 AB A silicon wafer characterized in that the laser scattering tomography defect occurrence region accounts for at least 80% of the wafer surface area and that the laser scattering tomography defects have a mean size of not more than $0.1 \mu\text{m}$, with the density of those defects which exceed $0.1 \mu\text{m}$ in size being not more than $1 \times 10^{5.5}$ cm⁻³, and wafers derived from this wafer as the raw material by heat treatment for oxide precipitate formation, by heat treatment for denuded layer formation or by epitaxial layer formation on the surface are useful as semiconductor materials.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2002:156842 USPAT2
 TI Silicon wafer and epitaxial silicon wafer utilizing same
 IN Murakami, Hiroki, Saga, JAPAN
 Egashira, Kazuyuki, Saga, JAPAN
 PA Sumitomo Metal Industries, Ltd., Osaka, JAPAN (non-U.S. corporation)
 PI US 6569535 B2 20030527
 AI US 2001-17295 20011218 (10)

PRAI JP 2000-387045 20001220
DT Utility
FS GRANTED
EXNAM Primary Examiner: Jones, Deborah; Assistant Examiner: Stein, Stephan
LREP Armstrong, Westerman & Hattori, LLP
CLMN Number of Claims: 18
ECL Exemplary Claim: 17
DRWN 11 Drawing Figure(s); 9 Drawing Page(s)
LN.CNT 956
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

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Your Search was:

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First Name = HIROSHI

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<u>08089522</u>	<u>5377266</u>	150	07/21/1993	SCRAMBLE APPARATUS AND DESCRAMBLE APPARATUS	TAKENO, HIROSHI
<u>08310754</u>	<u>5636279</u>	150	09/23/1994	SCRAMBLE APPARATUS AND DESCRAMBLE APPARATUS	TAKENO, HIROSHI
<u>08358597</u>	<u>5604499</u>	250	12/14/1994	VARIABLE-LENGTH DECODING APPARATUS	TAKENO, HIROSHI
<u>08364095</u>	<u>5568140</u>	150	12/27/1994	HEADER DETECTOR AND ASSOCIATED DECODING APPARATUS	TAKENO, HIROSHI
<u>08379900</u>	<u>5625355</u>	150	01/27/1995	APPARATUS AND METHOD FOR DECODING VARIABLE-LENGTH CODE	TAKENO, HIROSHI
<u>08524453</u>	<u>5598452</u>	250	09/06/1995	METHOD OF EVALUATING A SILICON SINGLE CRYSTAL	TAKENO, HIROSHI
<u>09188468</u>	<u>6206961</u>	150	11/09/1998	METHOD OF DETERMINING OXYGEN PRECIPITATION BEHAVIOR IN A SILICON MONOCRYSTAL, METHOD OF DETERMINING A PROCESS FOR PRODUCING SILICON MONOCRYSTALLINE WAFERS, AND RECORDING MEDIUM CARRYING A PROGRAM FOR DETERMINING OXYGEN PRECIPITATION BEHAVIOR IN A SILICON MONOCRYSTAL	TAKENO, HIROSHI
<u>09321567</u>	<u>6277715</u>	250	05/28/1999	PRODUCTION METHOD FOR SILICON EPITAXIAL WAFER	TAKENO, HIROSHI

<u>09345098</u>	<u>6143071</u>	150	06/30/1999	METHOD FOR HEAT TREATMENT OF SILICON SUBSTRATE, SUBSTRATE TREATED BY THE METHOD, AND EPITAXIAL WAFER UTILIZING THE SUBSTRATE	TAKENO, HIROSHI
<u>09529661</u>	<u>6478883</u>	150	04/18/2000	SILICON SINGLE CRYSTAL WAFER, EPITAXIAL SILICON WAFER, AND METHODS FOR PRODUCING THEM	TAKENO, HIROSHI
<u>09648180</u>	<u>6264906</u>	150	08/25/2000	Method for heat treatment of silicon substrate, substrate treated by the method, and epitaxial wafer utilizing the substrate	TAKENO, HIROSHI
<u>09830386</u>	<u>6544332</u>	150	04/26/2001	METHOD FOR MANUFACTURING SILICON SINGLE CRYSTAL, SILICON SINGLE CRYSTAL MANUFACTURED BY THE METHOD, AND SILICON WAFER	TAKENO, HIROSHI
<u>09869932</u>	<u>6544490</u>	150	07/09/2001	SILICON WAFER AND PRODUCTION METHOD THEREOF AND EVALUATION METHOD FOR SILICON WAFER	TAKENO, HIROSHI
<u>09926202</u>	Not Issued	135	09/24/2001	Method for producing silicon epitaxial wafer	TAKENO, HIROSHI
<u>10019298</u>	<u>6544899</u>	150	01/04/2002	PROCESS FOR MANUFACTURING SILICON EPITAXIAL WAFER	TAKENO, HIROSHI
<u>10380975</u>	<u>6858094</u>	150	03/20/2003	SILICON WAFER AND SILICON EPITAXIAL WAFER AND PRODUCTION METHODS THEREFOR	TAKENO, HIROSHI
<u>10482099</u>	Not Issued	71	12/24/2003	Method of producing annealed wafer and annealed wafer	TAKENO, HIROSHI
<u>10482843</u>	<u>7033962</u>	150	01/06/2004	METHODS FOR MANUFACTURING SILICON WAFER AND SILICONE EPITAXIAL WAFER, AND SILICON EPITAXIAL WAFER	TAKENO, HIROSHI

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<u>10501672</u>	Not Issued	30 <i>Applicants</i>	07/16/2004	Silicon epitaxial wafer and its production method	TAKENO, HIROSHI
<u>10530557</u>	Not Issued	20	04/07/2005	Annealed wafer and method for manufacturing the same	TAKENO, HIROSHI
<u>11339672</u>	Not Issued	25	01/26/2006	Methods for manufacturing silicon wafer and silicon epitaxial wafer, and silicon epitaxial wafer	TAKENO, HIROSHI
<u>08982408</u>	<u>6101191</u>	150	12/02/1997	NETWORK CONNECTION CIRCUIT	TAKENOSHITA, HIROSHI
<u>09959730</u>	<u>6448500</u>	150	11/05/2001	BALANCED TRANSMISSION SHIELDED CABLE	TAKENOSHITA, HIROSHI
<u>08760214</u>	Not Issued	161	12/04/1996	POLYPROPYLENE RESIN COMPOSITION	TAKENOUCHI, HIROSHI
<u>09109936</u>	Not Issued	161	07/02/1998	POLYPROPYLENE RESIN COMPOSITION HAVING IMPROVED IMPACT STRENGTH AND RIGIDITY	TAKENOUCHI, HIROSHI
<u>09963529</u>	<u>6586531</u>	150	09/27/2001	POLYOLEFIN MASTERBATCH AND COMPOSITION SUITABLE FOR INJECTION MOLDING	TAKENOUCHI, HIROSHI
<u>10506950</u>	Not Issued	71	09/08/2004	Polyolefin masterbatch for preparing impact-resistant polyolefin articles	TAKENOUCHI, HIROSHI
<u>11138943</u>	Not Issued	41	05/25/2005	Heater for heating a wafer and method for fabricating the same	TAKENOUCHI, HIROSHI
<u>60237364</u>	Not Issued	159	10/04/2000	Polyolefin masterbatch and composition suitable for injection molding	TAKENOUCHI, HIROSHI

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